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A GaAs Microwave MESFET with Extremely Low Distortion

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Abstract

A ku-band GaAs power FET with extremely low signal distortion was fabricated on a material with graded doping profile, grown by a special vapor phase epitaxy technique. The device has a nearly constant g_m over a wide range of the bias. At P_o = 18 dBm and P_{sat} = 24 dBm power levels of a 6 to 18 GHz broad band amplifier, this device demonstrates second harmonic levels as low as 40 dBc and 22 dBc, respectively, which is the lowest ever reported.

Introduction

GaAs microwave MESFETs with graded channel doping profiles have been studied extensively in the past decade due to their superior RF performance and, especially, the output signal linearity [1] - [7]. Unlike devices with uniform channel doping profiles, the transconductance, g_m, of graded channel doping devices does not drop rapidly as the gate to source bias, V_{gs}, increases. This unique property greatly improves the output signal linearity for large signal applications. For low noise applications, a higher g_m can be maintained near pinchoff, which yields a lower noise figure since g_m is inversely related to the noise figure.

This paper presents a ku-band medium power FET with an extremely low signal distortion by using a graded doping material. The multi-layer material structure, grown by a special VPE technique, will be described first, followed by a brief description of the device fabrication process. The DC parameters and RF performance of this device then will be presented. Finally, a method that predicts the second harmonic distortion at a given output power level will be discussed in brief.

Material Structure And Device Fabrication

Fig. 1 shows the doping profile of the material for this device. The multi-layer structure, grown by an $AsCl_3$ vapor phase reactor, consists of a highly doped (>10^{18} cm^{-3}) contact layer for low ohmic contact resistance, a lightly doped (~10^{16} cm^{-3}) separation layer, a medium doped (4-7x10^{17} cm^{-3}) active layer and an undoped buffer layer. The thickness of each layer was well controlled to achieve the reproducible device characteristics. The abrupt transition in the doping level from the active layer to the separation layer was accomplished with a unique set of growth conditions. This abruptness in the doping transition was found to be critical for the linearity of the device performance.

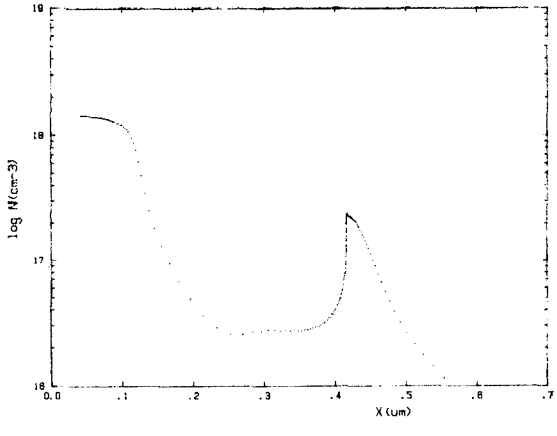

Fig. 1
Graded channel doping profile

To fabricate the MESFET on the graded doping material, the mesa was first formed by a wet etching. Au-Ge/Ni/Au was deposited and alloyed to provide the drain/source ohmic contact. After the highly doped contact layer was etched away

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to form the recess channel, the 0.5 x 280 um^2 Ti/Pt/Au gate was deposited onto the lightly doped separation layer. Fig. 2 shows the cross section of this device. The amount of the recess was experimentally optimized to achieve both high and linear g_m.

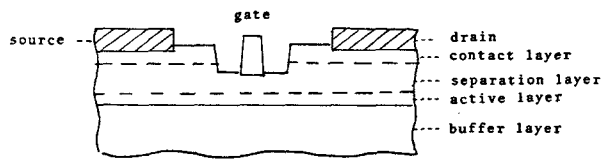

Fig. 2
Cross-section of the device with graded channel doping profiles

DC Parameters and RF Performance

Fig. 3(a) and 3(b) show the g_m and I_{ds} vs. V_{gs} curves of this device. Note that the g_m is nearly constant over a wide range of V_{gs}. For comparison Fig. 3(c) shows the g_m and I_{ds} vs. V_{gs} curves of a uniformly doped device. The device has an I_{dss} around 100 mA, a g_m of about 32 ms and a V_p = 3.5 to 5.5 volts. The gate to drain and gate to source break-down voltages are around 20 volts. These break down voltages are better than those of uniformly doped devices with the same geometry and I_{dss} density, because the gate of the graded doping device is placed on a low doping separation layer. The gate capacitance, C_{gs}, also appears to be lower for this device due to the low doping layer underneath the gate.

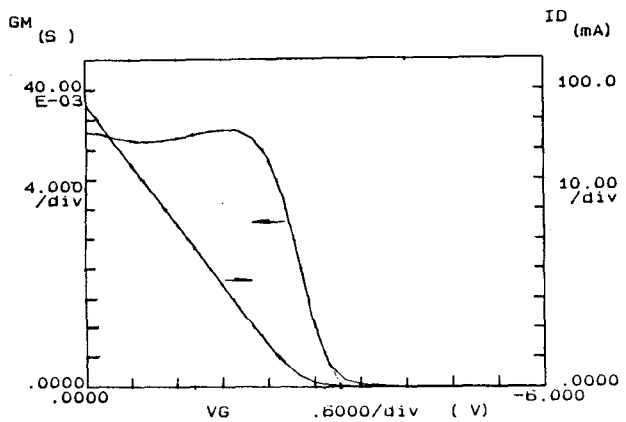

Fig. 3(a)
g_m and I_{ds} vs. V_{gs} for the device with graded channel doping profile. Note that g_m is rather flat over a large range of the gate bias.

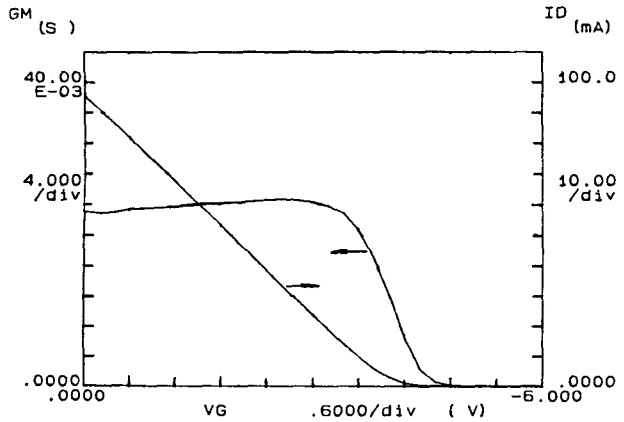

Fig. 3(b)
Same as Fig. 3(a)

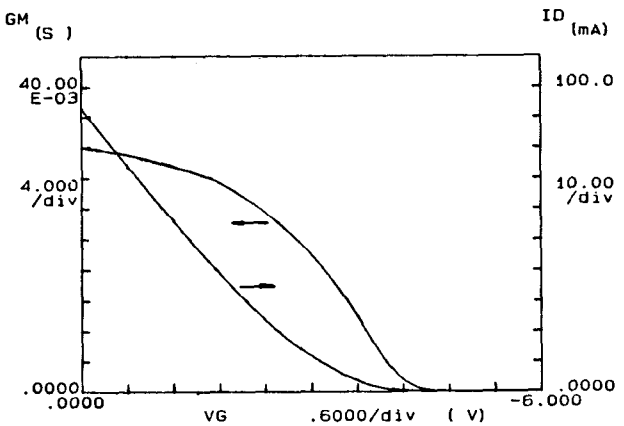

Fig. 3(c)
g_m and I_{ds} vs. V_{gs} for device with uniform doping profile. Note that g_m drops rather rapidly as V_{gs} increases

At 18 GHz this device demonstrates 7 dB gain and 20.5 dBm output power at the 1 dB compression point for V_{ds} = 6 volts and I_{ds} = 1/2 I_{dss}, comparing to 5 dB gain and 19.5 dBm power of a conventional device with the same geometry. At the power bias point this device's noise figure is 7 dB, also better than conventional FETs by about 2 dB. The power added efficiency at 18 GHz for this device is 30.67% comparing to 20.31% for conventional devices. The better RF performance of this device is attributed to its higher g_m value at the gate bias point and its much better g_m linearity which raises the 1 dB compression point and improves its output power limiting characteristics.

A 6 to 18 GHz broad band balanced amplifier module, using a pair of these devices, demonstrates 6 dB gain and 22 dBm power across the band. At P_o = 18 dBm and

P_{sat} = 24 dBm, the second harmonic levels are as low as 40 dBc and 22 dBc, respectively. We believe that a such low second harmonic distortion level has not been previously reported in the literature. Table 1 compares the measured second harmonic distortion at two output power levels for the graded doping device and a uniformly doped device.

	Graded Doping Device	Uniform Doping Device
S.H. level at P_o=18 dBm	40 dBc	22 dBc
S.H. level at P_{sat}=24 dBm	22 dBc	10 dBc

Table 1
Comparison of the second harmonic levels at P_o = 18 dBm and P_{sat} = 24 dBm between graded doping devices and uniform doping devices. The unit "dBc" represents the distance in dBm between the power level of the carrier frequency and the second harmonic level.

Prediction of the Second Harmonic Level

Similar to the method in [2] we derived a simple method to estimate the second harmonic level at a given output power level from the DC transfer characteristic of a device. A least squares quadratic

$$g_m(V_{gs}) = g_{mo} + g_{m1} V_{gs} + g_{m2} V_{gs}^2 \quad \text{Eq. 1}$$

was to fit to the g_m vs. V_{gs} characteristics. g_{mo} is the g_m at V_{gs} = 0. g_{m1} and g_{m2} can be found by fitting Eq. 1 into at least two V_{gs} points.

Integration of Eq. 1 gives the cubic approximation of I_{ds} vs. V_{gs} curve

$$I_{ds} = I_{dss} + g_{mo}V_{gs} + \frac{g_{m1}}{2} V_{gs}^2 + \frac{g_{m2}}{3} V_{gs}^3 \quad \text{Eq. 2}$$

where I_{dss} is integration constant, which equals the drain saturation current.

To translate the reference point of the gate voltage from V_{gs} = o to the DC bias point V_{gb}, let

$$\tilde{V}_{gs} = \pm V_{gb} \mp V_{gs} \quad \text{Eq. 3}$$

where $\tilde{V}_{gs}$ is the voltage swing around the DC bias point V_{gb}. The different signs in the equation correspond to the two swing directions.

Eq. 3 can be re-written as

$$V_{gs} = V_{gb} \mp \tilde{V}_{gs} \quad \text{Eq. 4}$$

substitute Eq. 4 into Eq. 2

$$I_{ds} = k_o \mp K_1 \tilde{V}_{gs} + K_2 \tilde{V}_{gs}^2 \mp K_3 \tilde{V}_{gs}^3 \quad \text{Eq. 5}$$

where $k_o = I_{dss} + g_{mo} V_{gb} + \frac{g_{m1}}{2} V_{gb}^2 + \frac{g_{m2}}{3} V_{gb}^3$;

$$k_1 = g_{mo} + g_{m1} V_{gb} + g_{m2} V_{gb}^2;$$

$$k_2 = \frac{g_{m1}}{2} + g_{m2} V_{gb};$$

$$k_3 = \frac{g_{m2}}{3} V_{gb}^3.$$

According to [8],

$$P_o = 10 \log \left\{ \left(\frac{K_1 A}{\sqrt{2}} \right)^2 R_L 10^3 \right\} \quad \text{Eq. 6}$$

$$P_{S.H.} = 10 \log \left\{ \left(\frac{K_2 A^2}{\sqrt{2}\,2} \right)^2 R_L 10^3 \right\} \quad \text{Eq. 7}$$

Where P_o is the output power of the carrier wave and $P_{S.H.}$ is the second harmonic level; A is the gate voltage swing corresponding to P_o; R_L is the load resistance.

The signs in front of the coefficients in Eq. 5 are not important in calculating $P_{S.H.}$ since they will be squared anyway.

For a given output power, with the knowledge of K_1 and K_2, A can be solved from Eq. 6. Substitute this A into Eq. 7, $P_{S.H.}$ can be found.

Table 2 compares the calculated and measured $P_{S.H.}$ at P_o = 18 dBm for the devices in Fig. 3(b) and Fig. 3(c).

	Graded Doping Device	Uniform Doping Device
Measured S.H. level at P_o = 18 dBm	40 dBc	22 dBc
Calculated S.H.Level at P_o = 18 dBm	36.8 dBc	26.2 dBc

Table 2
Comparison between measured and calculated second harmonic levels for graded doping device and uniform doping device at P_o = 18 dBm.

Conclusion

A medium power FET with an extremely low signal distortion was developed by using a graded doping material. The unique property of this device makes it suitable for very low distortion broad band amplifier applications, as well as class B amplifiers. In addition, a method to predict the second harmonic level was presented and the calculated results agreed well to the measured values.

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